Avionics Systems On A Chip for Space Exploration

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Abstract. The advanced miniaturization of all the on-board spacecraft functions into a highly integrated, modular, and reliable architecture is a major enabling technology for future deep-space and Earth orbiting science missions. Avionics miniaturization using advanced deep sub-micron semiconductor digital, analog, as well as Micro Electro Mechanical Systems (MEMS) technologies will revolutionize the way we build future spacecraft systems. So called micro and nano satellites as well as other micro-systems are possible using these advanced technologies. In this paper, we present an overview of work in progress at the newly established JPL Center for Integrated Space Microsystems (CISM) in the area of Avionics Systems On a Chip Program. This long-term research and development program has been established as part of NASA's Advanced Deep Space Systems Program (a.k.a. X2000), which also has a near-term project-oriented element, as well as an even longer term research component called Revolutionary Computing Technologies. This paper will outline the vision, goals and scope of the SOAC program, as well as its target mission insertion opportunities. We also describe a technology roadmap from 1998 to 2006 leading to Systems On A Chip technology elements. Also described are the SOAC technology challenges and research components. The first SOAC prototype has been designed and submitted for fabrication at the MIT/LL 0.25 micron Silicon On Insulator (SOI) foundry in July 1998. It contains a telecommunications unit, power management unit, on-chip computer, non-volatile as well as volatile storage, all on a single chip. The chip will be tested at JPL in the second quarter of 1999.

INTRODUCTION

The design and development of advanced highly integrated, reliable, autonomous, and highly miniaturized micro-systems is a major enabling technology for future deep-space and Earth orbiting space exploration missions (Alkalai, 1998a and Alkalai, 1998b). Moreover, this technology is obviously applicable to all four NASA enterprises: Space Science, Earth Science, Human Exploration and Development of Space, and Aeronautics. Highly integrated microelectronics is also the major enabling technology behind the commercial consumer microelectronics revolution. This now makes the space microelectronics roadmap consistent with the trends in the commercial semiconductor industry. In particular, avionics *Systems On A Chip* solutions, which integrate multiple subsystem functions onto a single integrated chip, are of strategic importance to both the avionics space industry as well as the commercial consumer industry. Both industries will benefit from integrated micro-systems that utilize the following technologies:

- deep sub-micron digital and analog as well as mixed-signal microelectronics technology;
- integrated embedded passive components for power electronics and communications miniaturization;
- integrated thin-film micro-magnetic technology for non-volatile storage, micro-transformers, etc.;
- low-power technologies, devices, circuit design techniques and low-power system architectures;
- integrated design methodologies using third party intellectual properties (IP) as building blocks;
- integrated high-performance processing and high-density storage technology;
- integrated communications with on-chip computing, storage, and power management;

- integrated sensors and microelectronics;
- design for testability, built-in self test;
- design for high-yield, high-reliability, and fault-tolerance;

For example, the technology developed to implement a *System On A Chip* design that integrates RF communications, processing, storage, and power management on a single chip, would be applicable to embedded space applications such as mobile rovers on Mars, and also applicable to the mobile portable communications consumer applications on ground.

In this paper we describe work in progress at the Jet Propulsion Lab's Center for Integrated Space Microsystems (CISM) Systems On A Chip (SOAC) Program. This program is an element of NASA's Deep Space Systems Development Program also known as X2000. The main purpose of the X2000 Program is to deliver advanced spacecraft systems technology every three year. The first delivery is scheduled for the year 2000, followed by a second delivery in 2003, third in 2006, and so on. The SOAC program is one of two research components of X2000; the other (smaller) research component is developing long-term revolutionary computing technologies beyond 2010. Some elements of the SOAC program will target mission insertion into the X2000 second delivery (2003), whereas other elements will mature in time for the third delivery (2006).

In the remainder of this paper, we first describe the vision behind the systems on a chip program. We then outline the program goals, schedule, and roadmap. Following this, we describe the research elements of the SOAC program, describing the main technology challenges. A first prototype of the SOAC vision has been designed in collaboration with a university team from the University of Illinois, Chicago. This 'pathfinder' prototype chip contains on a single chip the following separate subsystem functions: power management and distribution, computing, volatile and non-volatile storage, and communications. This chip has been designed and fabricated using 0.25 micron Silicon On Insulator (SOI) technology, at the advanced semiconductor foundry at MIT/LL. Future designs of the SOAC prototype designs will include on-chip sensing capabilities as well as Micro Electro Mechanical Systems (MEMS). There are many anticipated applications of systems on a chip. From micro-rovers and micro-surface explorers, to highly redundant inflatable smart micro-structures, planetary micro-satellites performing cooperative planetary exploration, free-flying magnetometers, and many more. It is expected that the SOAC program will enable many new spacecraft system concepts that have not been considered in the past. X2000 Avionics Delivery Technology Roadmap.

SYSTEMS ON A CHIP LONG TERM VISION

Early in the program definition phase of the *System On A Chip* program (in early FY 1997), a vision was proposed of a highly integrated avionics system on a chip consisting of the following integrated subsystem functions:

- on-board computing (CPU)
- non-volatile and volatile storage (Mass Storage)
- RF communications (COM)
- power management and distribution for low-power architectures (PMAD)
- on-board Active Pixel Sensing (APS), for imaging and navigation and control.

This vision is schematically depicted in Figure 1 below. At the time, it was not clear how large such a chip would be, or whether the technology challenges required to implement this vision were overly ambitious.

RF com   power bus

S/C I/O

DMA
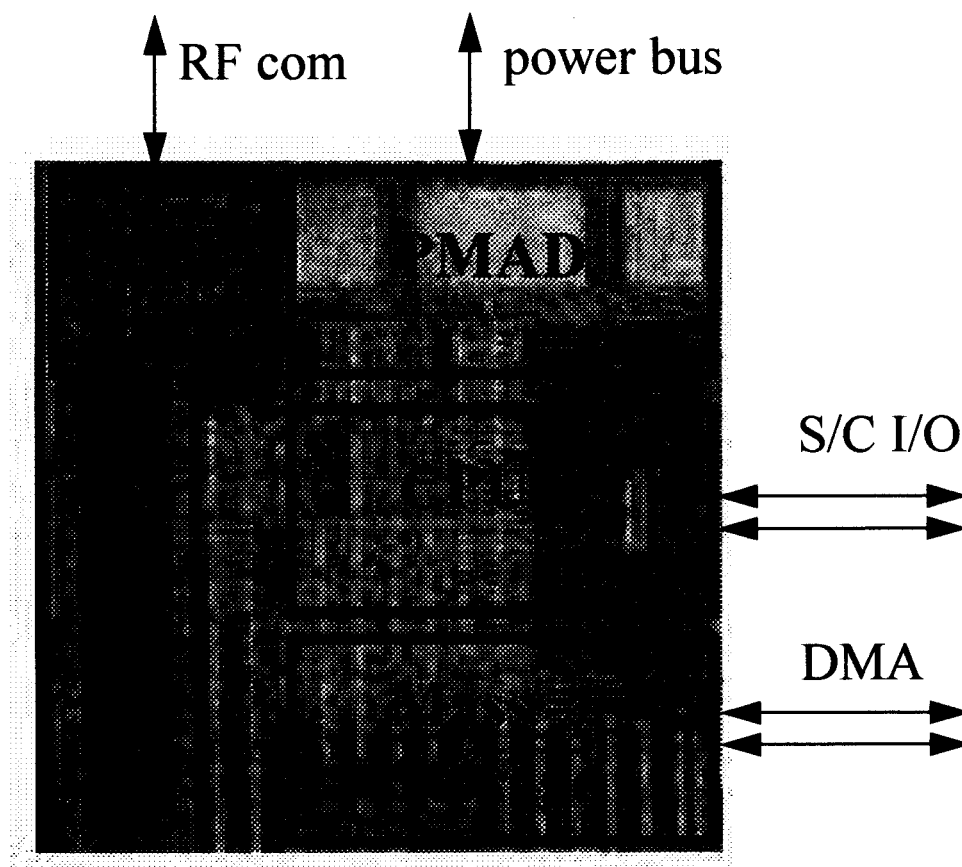
FIGURE 1. System on a chip concept.

TABLE 1. below, we show a space microelectronics technology roadmap that shows the target technologies in time for the 1st Avionics Delivery (year 2000), 2nd Avionics Delivery (2003), and the 3rd Avionics Delivery. The System On A Chip design will utilize the technologies for 2nd and 3rd deliveries.

Technology	1st Delivery (2000)	2nd Delivery (2003)	3rd Delivery (2006)
Semiconductor			
feature size	0.25m – 0.35m	0.18m – 0.25m	0.13m – 0.18m
process type	Bulk and SOI CMOS	SOI PD CMOS	SOI FD CMOS, SiGe
supply voltage	3.3 volts	2.5 volts	1.5 volt
LM (wafer size)	3-4 (6" – 8")	4-5 (8" – 10")	5-6 (10" – 12")
RH Building Blocks			
CPU	Power PC 750	Power PC Core	Standard Cell
SRAM	4 Mbit	16 Mbit	64 Mbit
ASIC	1.0 – 1.5 M gates	1.5 - 4.0 M gates	4.0 - 8.0 M gates
DRAM	64 Mbit	256 Mbit	1 Gbit
Flash, MRAM	64 Mbit	256 Mbit	1 Gbit
COTS Interfaces			
Local Bus	PCI 2.1 @66 Mhz,64-b	High-Rel PCI	On-Chip PCI
Low Power Utility Bus	I2C	I2C	Distributed I2C
Eng. Bus	1394 100 Mbps	LP 1773: 20 Mbps @ 0.2 watts/node	Multi-fiber optic links
High-Speed Bus	IEEE 1394	Low Power 1394	Macro Cell
Test Bus	IEEE 1149.1 JTAG	IEEE 1149.1/5 JTAG	Macro Cell
Advanced Packaging			

3D MCM Stack	Stnd. 4"x4" slices	Stnd. 2"x2" slices	Macro Cells in 3D chip stacks
3D Chip Stacking	48-high stacks	50-100 high stacks	3D VLSI
Design Automation			
CAD	VHDL Models	System-Level Models	System Synthesis
Collaborative Eng.	Distributed Design	Virtual Skunk-works	Language to Layout
Attitude Control			
Star Tracker	Adv. Stellar Compass	Optical Processing	Integrated msystem
Sun Sensors/Gyros/Acc.	MEMS-based	MEMS-based	MEMS-based
Fault Tolerance			
FT Model	Distributed FT	Distributed FT	Distributed FT
SW FT Model	SW implemented FT	Design for Reliability	Design for Yield
Techniques	Adaptive FT	Self Repair	Evolving
Reliability Modeling	Partial Models	Integrated Tools Set	End-to-End Models
Power Electronics			
PASM	16 switches, HDI	48 Switches HDI	Switches on chip
PMAD	High Efficiency DC/DC	PMAD/PASM	PMAD on a Chip
Telecom Processing			
Optical	I/F to Avionics	Optical Com in Stack	On Chip Interface
RF	STM	RF in the Stack	Telecom on a Chip
Advanced Processing			
Neural Networks	Autonomy support	S/C Navigation	Learning Cells
DSPs	SHARC21060 – HDSP	Ultra SHARC	Standard Cell
Optical Processing	Image Correlation	Precision Landing	On-Chip Support

## SOAC TECHNOLOGY DEVELOPMENT ELEMENTS

To support the development of avionics system on a chip technologies for NASA's space missions, following program elements were established: Deep space RF communication front end; Micro Inertial Reference System (mIRS); Active Pixel Sensors; Integrated Passive Components; System Integration, Architecture, Fabrication and Test; and Reliability.

## Deep space RF communication front end

The front end of the Telecommunication subsystem is a major area in which major mass (factor of 10) and volume (factor of 100) reduction can be found via the development of new silicon based micromachining technology and devices. Our objectives are to develop the main components that comprise a communication front end and integrate them in a single module which we refer to as a "cube". The major components include: single-pole double- throw switches, diplexer and solid state power amplifier (SSPA) . Silicon based technologies are being pursued because:

- Compatibility with silicon process translates to lower manufacturing cost
- Enables multiple RF and digital functions to be integrated together
- Compatibility with future advanced silicon digital technology
- Employing a single material baseline enables easier integrated of a multi-stack "cube" system
- Enables many System On A Chip architectures

Currently, The University of Michigan (UofM) is developing the MEMS based switch and compact diplexer (Drayton, 1998 and Pacheco, 1998) Fig. 2. For this year, two types of MEMS switch topologies are being investigated. Based on the final results, the best characteristics of both switches will be combined for a final optimize device design. The ultra small diplexer uses MEMS compatible (silicon based) high Q resonator technology. This forms the basis of a filter design. Based on this data, different filter topologies using the new technology will be studied in order to access how close we can come to achieve our performance goals.
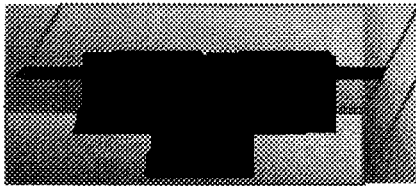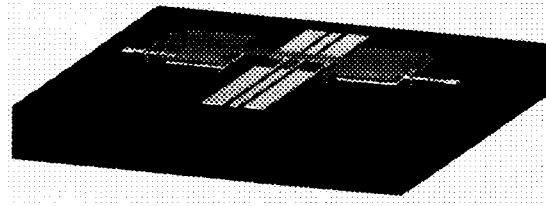
(a) RF high Q filer   (b) RF Switch

FIGURE 2. MEMS based RF component technology.

Until recently, there was a common perception that only III-V compounds could only be used for RF high power and low noise. However, advanced silicon heterojunction technology has broken into the low GHz regime and the ability to go higher is possible (Rieh, 1998) Therefore, we are investigating the use of SiGe for SSPA applications at 8.4 GHz and 32 Ghz.

Micro Inertial Reference System (mIRS)

Present navigation, guidance, and attitude control systems that use conventional gyroscope technologies are exceedingly costly, massive, and consume too much power for microspacecraft applications. The goal of this program is to develop new micromachined vibratory gyroscopes and accelerometers to replace conventional technology in a new micro Inertial Reference System (mIRS) for microspacecraft navigation, guidance, and attitude control applications (Tang, 1997 and Tang, 1996). The mIRS which consists of integrated micromachined gyroscope (Fig. 3), accelerometer, and control electronics will be used for attitude and maneuver control, and stabilization and pointing of instruments such as cameras, antenna, detectors, and solar panels. The mIRS can also supplement other external inertial reference systems such as the Global Positioning System (GPS), sun sensor, or star tracker by "filling in the gaps" during times the direct use of these systems is not possible. The silicon vibratory microgyroscope and accelerometer are fabricated using simple, precise, and low-cost bulk silicon machining technology. Currently, JPL microgyroscopes have consistently demonstrated a bias stability of < 30 deg/hr, and a rate random walk of < 2 deg/vhr with open-loop electronics and no temperature compensation.

The integrated micro Inertial Reference System offers potential advantages of long operational life, high performance, extremely compact size, low power operation, and low cost for applications in inertial navigation and attitude control of microspacecraft. Continual improvement and optimization of the clover leaf microgyroscope will result in performance of less than 1deg/hr bias stability in the near future.

Active Pixel Sensors

The goal of the program is to develop a CMOS based active pixel sensors (APS) that are compatible with the integration of on chip signal processing. Currently the program concentrates on the development of APS based imaging system which has high update rates , simultaneous multi-window access, digital filtering, and on-chip. Low power accurate computation of centroid from a predefined window in an image plane is required for many applications in space which includes star-trackers, rover navigation, and optical communication. Using a ultra-low power CMOS APS that features on-focal-plane computation of centroid, an order of magnitude improvement in speed and two orders of magnitude reduction of power over conventional CCD technology can be achieved, while miniaturizing the entire computational imaging system Fig. 4.
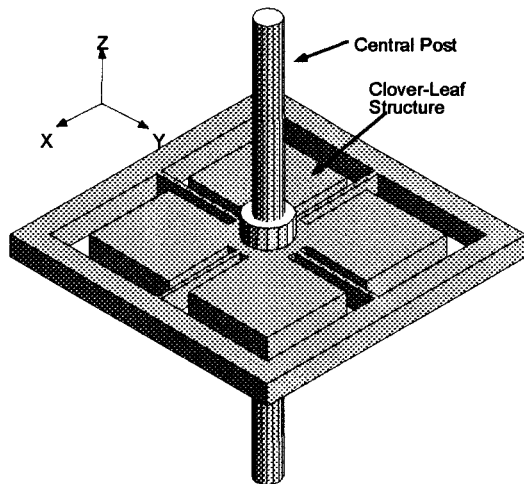
**FIGURE 3.** Schematic drawing of the microgyro structure.
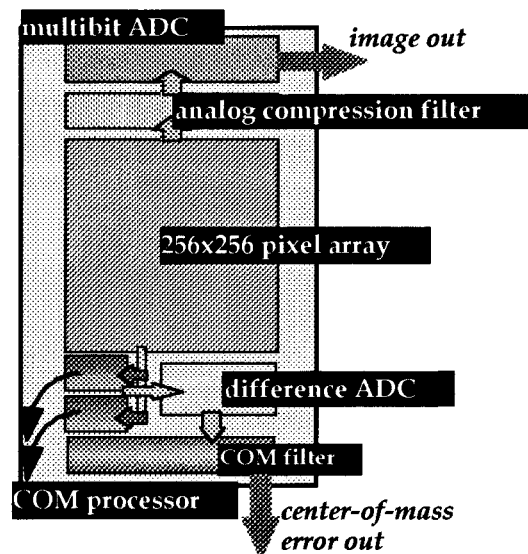
FIGURE 4. Low power CMOS APS imager on a chip.

Integrated Passive Components

Providing a power conversion system for the 'Systems on a Chip' (SOAC) program will require significant new technology. The diversity of voltage and current requirements for different subchips, the severe mass and volume constraints and the stringent power isolation requirements drive this new technology development. Particular effort is required to bring the inductors and transformers "on-chip". Inductors are used in conventional DC-DC converters for filtering and for energy transfer and storage. Microtransformers may be used to provide impedance matching and load isolation. Load isolation from a DC-DC converter is necessary to avoid DC ground loops, transfer of EMI to the loads, and interactions between the loads. If a load becomes shorted, the isolation transformer prevents the fault from reflecting back into the converter. Nevertheless, both Cassini and X2000 first delivery have had to forego load isolation because sufficiently compact transformers were not available. Compact, integratable, high frequency power supplies could enable robust, flexible power architectures. High frequency conversion increases the power density of the system and also entails the use of lower value passive components, making their on-chip fabrication feasible. Integrated components may, indeed, be necessary in order to provide the tight control over parasitic impedances which is vital to high frequency operation. Miniaturization obviously cuts the mass penalty of redundant power supplies. Miniaturization and integration also allow us to consider a distributed power architecture. Such an architecture might be realized with a primary 28 V power source, distributed at 15 V, interfacing to 1 W on-chip 1-10 MHz dc-dc converters which would supply 2, 3.3, or 5 V as needed. Magnetic materials must be incorporated with other components onto silicon for further integration of the power electronics and may enable higher frequency, higher power density power conversion. Integration of transformers and inductors with other active and passive components is one of the outstanding hurdles for developing an on-chip distributed power system. SOAC program is currently focusing on the development of miniaturized, thin-film based microtransformers, inductors, capacitors (with U. of Arkansas) and novel power system architectures.

System Integration, Architecture, Fabrication and Test

The overall objective of this task is to develop silicon chips that implement system level functions for integration into X2000's future flight hardware. Implementing systems on a chip for future space missions will require the buildup of an infrastructure that includes the proper design and verification tools, design flow and sign-off procedures, packaging, test, and flight qualification procedures. To reach these objectives in a timely manner for near-range missions (3-5 years), it is desirable to inherit base architectures, software and interfaces from verified systems that have been utilized on earlier missions (ie. X2000 first delivery). By utilizing JPL-developed one-of-a-kind sensors and cores in addition to cores procured from industry, the baseline functionality inherited from
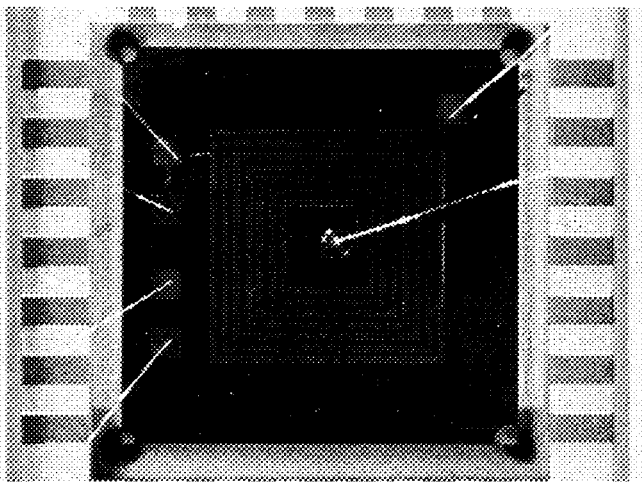
FIGURE 5. On-chip inductor.
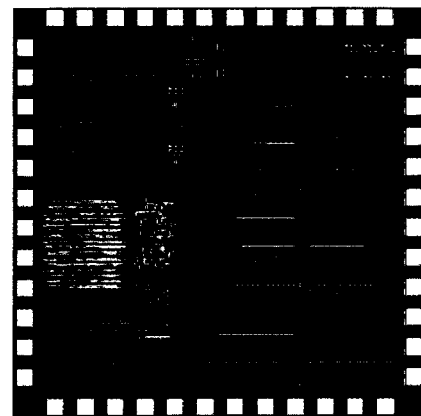
FIGURE 6. System on a chip prototype design.

previous missions would be maintained but with enhancements in performance and advanced capability to support new mission concepts. On the other hand, long-range missions (> 5 years) that implement radically new mission concepts may be driven by the new capabilities and architectural possibilities provided by the system-on-a-chip approach and would therefore inherit less from the systems of earlier missions. The first System on a Chip prototype design was submitted in July to MIT/LL for fabrication on the FDSOI CMOS (0.25 micron) line as part of the DARPA sponsored multiproject run (Fig. 6).

This design was generated in collaboration with the University of Illinois at Chicago (UIC). The FDSIO design was primarily generated through direct translation from a UIC design developed as a class project and submitted through MOSIS on AMI's 1.2-micron bulk CMOS process. Enhancements for testability and technology differences were incorporated into the prototype chip design. The prototype (2.6 mm by 2.6mm) includes a simple CPU, SRAM, power management and distribution, clock, and a UHF (400MHz) transceiver. A second test chip (2mm by 2mm) was also submitted for fabrication on the MIT/LL foundry run. This chip contains drop-out circuits from the prototype design and test structures used for process and device characterization. The goal of this design exercise was for the team to gain experience in System on a Chip design, integration and test needs for future collaboration with industry and academia in developing a full scale Avionics System on a Chip. In future work, emphasis will be placed on system architectures, development and integration of IP cores, foundries and design tools, testing capability, and on defining requirements for a mIRS core, an APS based star tracker /smart vision system core, and other sensor cores.

RELIABILITY

The reliability program address and solve reliability problems related to SOAC integrated circuits: stress induced voiding, electromigration, oxide breakdown, radiation damage and focuses on the development of new techniques for reliability and yield improvements. It addresses the effects of space environments on micromechanical properties and failure resistance of submicron circuits (Caltech) as well as the layout design techniques for reliability improvements of system on a chip.

CONCLUSIONS AND FUTURE PLANS

We have described the research and development at JPL Center for Integrated Space Microsystems leading to the "avionics system on a chip". This is a long-term project with a maturity time frame of 5-10 years. We will be working closely with universities and commercial foundries to develop monolithic and/or heterogeneous, highly integrated system on a chip solutions for science instruments and avionics, communication, and navigation systems.

ACKNOWLEDGMENTS

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